Claims

I claim:

1. An integrated circuit device, comprising:

a substrate having a trench formed therein;

an isolation layer disposed in the trench so as to cover a first sidewall portion of the trench; and

a gate electrode disposed on a second sidewall portion of the trench.

2. The integrated circuit device of Claim 1, further comprising:

a gate insulating layer disposed between the gate electrode and the second sidewall portion of the trench.

3. The integrated circuit device of Claim 1, further comprising:

a buffer layer disposed between the isolation layer and the trench.

4. The integrated circuit device of Claim 3, wherein the buffer layer comprises silicon oxide.

5. The integrated circuit device of Claim 3, further comprising:

a liner layer disposed between the isolation layer and the buffer layer.

6. The integrated circuit device of Claim 1, wherein the second sidewall portion of the trench comprises an impurity layer.

7. The integrated circuit device of Claim 6, wherein the impurity layer comprises boron dopant.

8. The integrated circuit device of Claim 1, wherein the substrate has a mesa formed thereon adjacent the trench that has an upper surface that intersects the second sidewall portion of the trench, and wherein a length of the second sidewall portion of the trench is at least 15% of a length of the upper surface.

9. The integrated circuit device of Claim 8, wherein the length of the second sidewall portion of the trench is approximately 30% - 60% of the length of the upper surface.

10. A method of manufacturing an integrated circuit device, comprising:

forming a trench in a substrate;

forming an isolation layer in the trench so as to cover a first sidewall portion of the trench; and

forming a gate electrode on a second sidewall portion of the trench.

11. The method of Claim 10, wherein forming the gate electrode comprises:

forming a gate insulating layer on the second sidewall portion of the trench; and

forming the gate electrode on the gate insulating layer.

12. The method of Claim 10, wherein forming the isolation layer comprises:

forming a buffer layer in the trench; and

forming the isolation layer on the buffer layer in the trench.

13. The method of Claim 12, wherein forming the isolation layer comprises:

forming a liner layer on the buffer layer; and

forming the isolation layer on the liner layer in the trench.

14. The method of Claim 10, further comprising:

forming an impurity layer in the second sidewall portion of the trench.

15. A method of manufacturing an integrated circuit device, comprising:

etching a substrate to form a trench and a mesa therein, the mesa comprising an upper surface and a sidewall, which is adjacent the trench;

filling the trench with an insulating material so as to cover a first portion of the sidewall and to expose a second portion of the sidewall; and

forming a gate electrode on the second portion of the sidewall and the upper surface.

16. The method of Claim 15, wherein the etching step comprises:

forming an oxide layer on the substrate;

forming a mask on the oxide layer;

patterning the mask to expose at least a portion of the oxide layer; and

etching the exposed portion of the oxide layer and the substrate to form the trench and the mesa.

17. The method of Claim 16, wherein filling the trench with the insulating material comprises:

filling the trench with the insulating material so as to cover the mask;

planarizing the insulating material until a surface of the mask is exposed;

patterning the insulating material so that the mask extends through a surface of the insulating material;

etching the mask to substantially remove the mask from the upper surface of the mesa; and

etching the insulating material so that the insulating material covers the first portion of the sidewall and exposes the second portion of the sidewall.

18. The method of Claim 15, further comprising:

forming a buffer layer in the trench before filling the trench with the insulating material; and

thermally treating the insulating material after filling the trench with the insulating material.

19. The method of Claim 15, further comprising:

implanting ion impurities in the second portion of the sidewall and the upper surface before forming the gate electrode.

20. The method of Claim 19, wherein implanting ion impurities comprises:

implanting ion impurities at an oblique angle with respect to a plane formed by a non-etched portion of the substrate in the second portion of the sidewall and the upper surface.

21. The method of Claim 15, wherein forming the gate electrode comprises:

forming an oxide layer on the second portion of the sidewall and the upper surface;

implanting ion impurities through the oxide layer in the second portion of the sidewall and the upper surface;

etching the oxide layer; and

forming the gate electrode on the second portion of the sidewall and the upper surface.

22. An integrated circuit device, comprising:

a substrate having a mesa structure thereon, the mesa structure having sidewalls and a top surface; and

a gate electrode on the mesa structure that extends across the top surface and down a portion of at least one of the sidewalls.

23. The integrated circuit device of Claim 22, further comprising:

a gate insulating layer disposed between the gate electrode and the portion of at least one of the sidewalls.

24. The integrated circuit device of Claim 22, wherein the portion of at least one of the sidewalls is a first portion of at least one of the sidewalls, the integrated circuitd device further comprising:

an isolation layer disposed on a second portion of at least one of the sidewalls.

25. A semiconductor device comprising:

a semiconductor substrate;

a trench which is formed by selectively etching the semiconductor substrate and which is partially filled with an isolation layer such that the upper sidewalls of the trench are exposed;

a gate insulating layer which is formed on upper sidewalls of the exposed trench and an upper surface of the semiconductor substrate; and

a gate electrode which is formed on the gate insulating layer.

26. The semiconductor device of Claim 25, further comprising a buffer layer which is formed at the interface between the isolation layer and the bottom and sidewall of the trench.

27. The semiconductor device of Claim 26, further comprising a liner of a silicon nitride layer which is formed at the interface between the buffer layer and the isolation layer.

28. The semiconductor device of Claim 25, wherein the surface of the isolation layer is lower than the upper surface of the semiconductor substrate.

29. The semiconductor device of Claim 25, further comprising an impurity layer for controlling threshold voltage which is formed under the surface of the upper sidewalls of the trench and the upper surface of the semiconductor substrate.

30. The semiconductor device of Claim 25, wherein the gate electrode covers the upper sidewalls of the trench and the surface of the isolation layer and is formed on the gate insulating layer which is interposed between the gate electrode and the upper surface of the semiconductor substrate.

31. A method of manufacturing a semiconductor device comprising the steps of:

forming a trench by etching a semiconductor substrate;

partially filling the trench with an isolation layer which leaves upper sidewalls of the trench exposed;

forming a gate insulating layer on the upper sidewalls of the exposed trench and an upper surface of the semiconductor substrate adjacent to the trench; and

forming a gate electrode on the gate insulating layer.

32. The method of manufacturing a semiconductor device of Claim 31 further comprising the step of forming a buffer layer at the interface between the isolation layer and the trench.

33. The method of manufacturing a semiconductor device of Claim 32 further comprising the step of forming a liner of a silicon nitride layer at the interface between the buffer layer and the isolation layer.

34. The method of manufacturing a semiconductor device of Claim 31, wherein the surface of the isolation layer is lower than the upper surface of the semiconductor substrate.

35. The method of manufacturing a semiconductor device of Claim 31, wherein the step of forming the isolation layer comprising the steps of:

forming a filling layer which fills the trench; and

etching the filling layer to a predetermined thickness so as to expose the upper sidewalls of the trench.

36. The method of manufacturing a semiconductor device of Claim 31, wherein the step of forming the trench comprises the steps of:

forming a pad oxide layer on the semiconductor substrate;

forming a mask on the pad oxide layer; and

etching the semiconductor substrate using the mask as an etching mask, and the step of forming the isolation layer comprises the steps of:

forming a filling layer which fills the trench;

chemically and mechanically polishing the filling layer so as to expose the surface of the mask;

etching the surface of the polished filling layer exposed by the mask;

removing the mask; and

etching the resultant filling layer so as to expose the upper sidewalls of the trench.

37. The method of manufacturing a semiconductor substrate of Claim 31 further comprising the step of forming an impurity layer to control threshold voltage beneath the surface of the upper sidewalls of the trench and beneath the upper surface of the semiconductor substrate before the step of forming the gate insulating layer.

38. The method of manufacturing a semiconductor substrate of Claim 37, wherein the impurity layer is formed using angle implantation.

39. The method of manufacturing a semiconductor device of Claim 31, wherein the gate electrode covers the upper sidewalls of the trench and the surface of the isolation layer and is formed on the gate insulating layer which is interposed between the gate electrode and the upper surface of the semiconductor substrate.